SEMICONDUCTOR DEVICE FOR APPLYING WELL BIAS AND METHOD OF FABRICATING THE SAME

ABSTRACT OF THE DISCLOSURE

A first conduction type well is formed in a substrate, and a second conduction type impurity region is formed in the well. A lower interlayer dielectric is formed on the substrate, including the well and the impurity region. A contact plug, connected to the impurity region through the lower interlayer dielectric, is formed with a void inside it. An upper interlayer dielectric is formed on the lower interlayer dielectric and the contact plug. The upper interlayer dielectric is selectively etched, forming an interconnection groove exposing the contact plug. The contact plug and the exposed void are overetched, extending the void into the first conduction type well. The interconnection groove is filled with a conductive layer, forming an interconnection. A seam extending to the well is formed in the void, connecting the contact plug to the well. Due to the seam, a well bias may be applied to the well.